Remarks

Claims 24-30 have been added. Claims 1-30 are now pending in the present application. Applicants respectfully request allowance of claims 1-30.

35 USC § 102 Claim Rejections

The Official Action mailed March 2, 2004 rejected claims 1-5, 7-10, 15-16, 18-19 and 21-22 as being anticipated by Spencer (U.S. Patent No. 6,295,582). Applicants believe this rejection has been overcome in view of the remarks that follow. Applicants respectfully request allowance of claims 1-5, 7-10, 15-16, 18-19 and 21-22.

As is well-established, in order to successfully assert a prima facie case of anticipation, the Official Action must provide a single prior art document that includes every element and limitation of the claim or claims being rejected. Therefore, if even one element or limitation is missing from the cited document, the Official Action has not succeeded in making a prima facie case.

Claim 7

Claim 7 recites

> 7. (Original) A mechanism to fetch data from a memory component, said mechanism comprising:
>
> a control unit to receive an indication regarding a frequency of a bus; and
>
> a storage device including a plurality of registers, each register to store parameters relating to data fetching based on a different frequency of said bus, said control unit to obtain said parameters

based on said indication, said control device to further fetch said data from said memory component based on said parameters.

Applicants' invention of claim 7 requires a storage device including a plurality of registers where each register stores parameters relating to data fetching based on a different frequency of a bus. Applicants respectfully submit that Spencer does not disclose such a plurality of registers. It appears that the Official Action relies on the flush control register 208 of Spencer for such a teaching. However, this is merely a single register and not a plurality of registers as required by claim 7. Furthermore, the flush control register 208 does not store parameters for fetching data that are based upon frequency of a bus. Spencer describes the contents of the flush control register 208 in detail in Table 1 and Table 2 of column 15. The parameters programmatically define a cache flushing policy but none of the disclosed parameters appear to be dependent upon or related to the frequency of the bus. In other words, Spencer doesn't teach that appropriate values for the parameters of the flush control register 208 are dependent upon the frequency of the bus or that it may be advantages to program the flush control register 208 with different parameters based upon the frequency of the bus.

However, Applicants' invention of claim 7 may enable tuning the process of fetching data from a memory component based upon the frequency of a bus. For example, an embodiment encompassed by the invention of claim 7 may store parameters for a first bus frequency (e.g. 33Mhz) in a first register and may store parameters for a second bus frequency (e.g. 66 MHz) in a second register. The control unit may receive an indication that the bus is operating at the second bus frequency (e.g. 66 MHz) and may fetch data from the memory component using the parameters of

the second register. Similarly, the control unit may receive an indication that the bus is operating at the first bus frequency (e.g. 33 MHz) and may fetch data from the memory component using the parameters of the first register. By using different parameters for each bus frequency, the mechanism may fetch data from the memory component more efficiently than if limited to a single set of parameters for all supported frequencies of the bus.

Applicants submit that Spencer does not disclose a storage device including a plurality of registers where each register stores parameters relating to data fetching based on a different frequency of a bus as required by the invention of claim 7. Since Spencer does not disclose each and every limitation of Applicants' claim 7, Spencer does not anticipate the invention of Applicants' claim 7. Applicants respectfully request allowance of claim 7.

Claim 8

Claim 8 further requires that the parameters relate to a data transfer size, thus resulting in the control unit fetching data based further upon the data transfer size. For example, an embodiment encompassed by the invention of claim 8 may store a parameter related to a first data transfer size (e.g. 2 cache lines) for a first bus frequency (e.g. 33Mhz) in a first register and may store a parameter related to a second data transfer size (e.g. 1 cache line) for a second bus frequency (e.g. 66 MHz) in a second register. The control unit may receive an indication that the bus is operating at the second bus frequency (e.g. 66 MHz) and may fetch data from the memory component using the parameter related to second data transfer size of the second register. Similarly, the control unit may receive an indication that the bus is operating at the first bus frequency (e.g. 33 MHz) and may fetch data from the memory component

using the parameter related to the first data transfer size of the first register. By using different parameters related to different data transfer sizes for each bus frequency, the mechanism may fetch data from the memory component more efficiently than if limited to a single set of parameters for all supported frequencies of the bus.

Spencer however does not disclose parameters relating to data fetching based on a different frequency that are also related to data transfer size as required by the invention of Applicants' claim 8. The Official Action points to Spencer at column 3, lines 13-14 for support of such a teaching. However, column 3, lines 13-14 merely states "determining the number of data bytes to be read into the cache memory (if more than one), and immediately reading all the requested data bytes into available cache memory space." However, Spencer does not appear to disclose that the number of data bytes to be transferred is based upon frequency of the bus or parameters defined for a bus having such a frequency as required by the invention of Applicants' claim 8.

Spencer does not anticipate the invention of Applicants' claim 8 since Spencer does not disclose each and every limitation of Applicants' claim 8. Applicants respectfully request allowance of claim 8.

Claim 9

Claim 9 further requires that the parameters relate to a threshold value, thus resulting in the control unit fetching data based further upon the threshold value. For example, an embodiment encompassed by the invention of claim 9 may store a parameter related to a first threshold value (e.g. 32 bytes) for a first bus frequency (e.g. 33Mhz) in a first register and may store a parameter related to a second threshold value (e.g. 64 bytes) for a second bus frequency (e.g. 66 MHz) in a second register. The control unit may receive an indication that the bus is operating at the second bus

frequency (e.g. 66 MHz) and may fetch data from the memory component using the parameter related to second threshold value of the second register. Similarly, the control unit may receive an indication that the bus is operating at the first bus frequency (e.g. 33 MHz) and may fetch data from the memory component using the parameter related to the first threshold value of the first register. By using different parameters related to different threshold values for each bus frequency, the mechanism may fetch data from the memory component more efficiently than if limited to a single set of parameters for all supported frequencies of the bus.

Spencer however does not disclose parameters relating to data fetching based on a different frequency that are also related to a threshold value as required by the invention of Applicants' claim 9. The Official Action points to the "predetermined amount" of Spencer for support of such a teaching. However, Spencer utilizes the "predetermined amount" to determine whether a cache memory has an adequate amount of free space. If the amount of free space in the cache memory drops below the predetermined amount, then Spencer flushes at least one line of data from the cache memory. (See, Spencer at column 3, lines 17-27). Accordingly, Spencer *flushes* data from the cache memory based upon the amount of free space falling below the predetermined amount. However, unlike the invention of claim 9, Spencer does not *fetch* data base upon a threshold value.

Spencer does not anticipate the invention of Applicants' claim 9 since Spencer does not disclose each and every limitation of Applicants' claim 9. Applicants respectfully request allowance of claim 9.

Claim 10

The invention of claim 10 requires a control unit to fetch an additional amount of data from the memory component at least based on a threshold value of the storage device. As stated above in regard to claim 9, Spencer discloses *flushing* based upon a predetermined value and does not disclose fetching based upon a threshold value as required by the invention of claim 10. Accordingly, Spencer does not anticipate the invention of claim 10. Applicants respectfully request allowance of claim 10.

Claims 15 and 16

Claim 15 requires a plurality of registers that each contain parameters corresponding to a different operating frequency of a bus. As stated above in regard to claim 10, Spencer merely disclose a single flush control register 208 and not a plurality of registers as required by claim 15. Spencer therefore does not anticipate the invention of claim 15. Claim 16 is dependent upon claim 15 and therefore is allowable for at least the reasons stated for claim 15. Applicants respectfully request allowance of claims 15 and 16.

Claim 18

Claim 18 requires a plurality of registers each to contain parameters corresponding to a different operating frequency of a bus (claim 16), wherein the parameters correspond to an initial request length, an initial threshold length, a subsequent request length, and a subsequent threshold length. The Official Action points to Spencer claim 1 for support. However, Spencer claim 1 does not disclose obtaining parameters corresponding to an operating frequency from a plurality of registers. Further, Spencer claim 1 does not disclose that the obtained parameters

correspond to an initial request length, an initial threshold length, a subsequent request length, and a subsequent threshold length.

Applicants' respectfully submit that the Official Action may have inadvertently mischaracterized the teaching of Spencer claim 1. In particular, the Official Action states "step (e) discloses a predetermined amount of space, which is the size of the initial request from memory when a peripheral request is accepted; thus, it is the initial request length." Step (e) merely determines whether the cache memory has a predetermined amount of empty space. The only correlation between the amount of empty space and a request length is that the cache memory should maintain enough empty space to store data received from a request. The predetermined amount could accommodate data for one or more requests and does not set the data size of the request. In particular, as indicated in Table 2, bits 0-1 of the flush control register 208 identify the amount of empty space to maintain.

Claim 19

The invention of claim 19 requires a data fetching mechanism to fetch an additional amount of data from the memory component at least based on a threshold value of the storage device. As stated above in regard to claim 9, Spencer discloses *flushing* based upon a predetermined value and does not disclose fetching based upon a threshold value as required by the invention of claim 19. Accordingly, Spencer does not anticipate the invention of claim 19. Applicants respectfully request allowance of claim 19.

Claims 1 and 21

Claims 1 and 21 require obtaining parameters based upon an operating frequency of a bus and fetching data based upon the obtained parameters. As discussed in detail in regard to claim 7, Spencer does not disclose obtaining parameters based upon the frequency of a bus, nor does Spencer disclose fetching data based upon the obtained parameters. Spencer merely discloses a cache memory that straddles two time domains where one side of the cache memory operates at one frequency and another side operates at another frequency. Spencer does not disclose that the bus frequency on either side may change nor does Spencer disclose adjusting the manner by which data is fetched into the cache memory based upon the frequency of the buses. In other words, Spencer fetches data from memory using the same manner regardless of the operating frequency of the bus and does not fetch data dependant upon parameters that were obtained based upon the operating frequency of the bus as required by claims 1 and 21. Applicants respectfully request allowance of claims 1 and 21.

Claims 2-5 and 22

Claims 2-5 and 22 depend from claim 1 and 21. Accordingly, claims 2-5 and 22 are allowable for at least the reasons discussed above. Applicants respectfully request allowance of claims 1 and 21.

35 USC § 103 Claim Rejections

Claim 17

The Official Action rejected Claim 17 under 35 U.S.C. 103(a) as being unpatentable over Spencer. Claim 17 depends from claim 15 and is therefore allowable

for at least one or more of the reasons stated above in regard to claim 15. Additional points could be made in support of the allowance of claim 17. However, Applicants believe the above is sufficient to overcome the present rejection of claim 17 under Spencer. Accordingly, such arguments will not be presented at this time so as to not burden the Examiner with the review of superfluous points. Applicants respectfully request allowance of claim 17.

Claims 6, 11-14, 20 and 23

The Official Action further rejected claims 6, 11-14, 20 and 23 under 35 U.S.C. 103(a) as being unpatentable over the combination of Spencer and Brown et al. (U.S. Patent No. 4,476,524). Claims 6, 11-14, 20 and 23 depend from one or more of claims discussed above. Accordingly, claims 6, 11-14, 20 and 23 are therefore allowable for at least one or more of the reasons stated above. Additional points could be made in support of the allowance of claims 6, 11-14, 20 and 23. However, Applicants believe the above is sufficient to overcome the present rejection of claim 6, 11-14, 20 and 23. Accordingly, such arguments will not be presented at this time so as to not burden the Examiner with the review of superfluous points. Applicants respectfully request allowance of claims 6, 11-14, 20 and 23.

Newly Added Claims

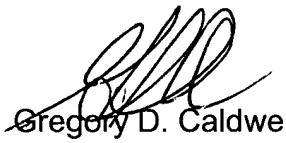
Claims 24-30 have been added and include novel and nonobvious limitations not taught by the cited art. For example, each of claims 24-30 require detecting operating characteristics of a bus, and selecting a parameter set from a plurality of parameter sets based upon the detected operating characteristics of the bus. Allowance of claims 24-30 is respectfully requested.

Conclusion

The foregoing is submitted as a full and complete response to the Official Action mailed September 17, 2003. Applicants submit that all pending claims are in condition for allowance. Reconsideration is requested, and allowance of the pending claims is earnestly solicited.

Should it be determined that an additional fee is due under 37 CFR §§1.16 or 1.17, or any excess fee has been received, please charge that fee or credit the amount of overcharge to deposit account #02-2666. If the Examiner believes that there are any informalities which can be corrected by an Examiner's amendment, a telephone call to the undersigned at (503) 439-8778 is respectfully solicited.

Respectfully submitted,



Gregory D. Caldwell
Senior Patent Attorney
Reg. No. 39,926

c/o Blakely, Sokoloff, Taylor & Zafman, LLP
1279 Oakmead Parkway
Sunnyvale, CA 94085-4040
(408) 720-8300